

CLAIMS:

1. A static random access memory cell comprising:

a first p-channel pullup transistor having a gate, drain, and source;

a first n-channel pulldown transistor having a gate, drain, and source;

a second p-channel pullup transistor having a gate, drain, and source;

a second n-channel pulldown transistor having a gate, drain, and source; the source of the first pullup transistor being adapted to be connected to a first voltage; the source of the second pullup transistor being adapted to be connected to the first voltage; the drain of the first pulldown transistor being connected to the drain of the first pullup transistor; the drain of the second pulldown transistor being connected to the drain of the second pullup transistor; the source of the first pulldown transistor being adapted to be connected to a second voltage lower than the first voltage; the source of the second pulldown transistor being adapted to be connected to the second voltage; the gate of the first pullup transistor being connected to the gate of the first pulldown transistor; the gate of the second pullup transistor being connected to the gate of the second pulldown transistor; the first pullup transistor and the first pulldown transistor together defining a first inverter having an output defined by the drain of the first pulldown transistor and an input defined by the gate of the first pulldown

1 transistor, the second pullup transistor and the second pulldown  
2 transistor together defining a second inverter having an output defined  
3 by the drain of the second pulldown transistor and an input defined by  
4 the gate of the second pulldown transistor, the input of the first  
5 inverter being connected to the output of the second inverter, and the  
6 input of the second inverter being connected to the output of the first  
7 inverter; and

8 a p-channel isolation transistor connected between the drain of the  
9 first pullup transistor and the drain of the second pullup transistor, and  
10 having a gate.

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12 2. A static random access memory cell in accordance with  
13 claim 1 wherein the source of the first p-channel transistor is connected  
14 to the source of the second p-channel transistor, and to the gate of the  
15 p-channel isolation transistor.

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17 3. A static random access memory cell in accordance with  
18 claim 1 wherein the p-channel isolation transistor comprises an active  
19 area that is common to both the first pullup transistor and the second  
20 pullup transistor.

1           4.    A static-random access memory cell in accordance with  
2 claim 1 wherein the source of the first pullup transistor is connected  
3 to the first voltage, wherein the source of the second pullup transistor  
4 is connected to the first voltage, wherein the source of the first  
5 pulldown transistor is connected to the second voltage, wherein the gate  
6 of the p-channel isolation transistor is connected to the first voltage,  
7 and wherein the source of the second pulldown transistor is connected  
8 to the second voltage.

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10           5.    A static random access memory cell in accordance with  
11 claim 1 wherein the p-channel isolation transistor comprises an active  
12 area that is common to both the drain of the first pullup transistor and  
13 the drain of the second pullup transistor.

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15           6.    A static random access memory cell in accordance with  
16 claim 1 and further comprising a first bit line; a second bit line; a  
17 word line; a first access transistor having a first active terminal  
18 connected to the output of the first inverter, having a second active  
19 terminal connected to the first bit line, and having a gate adapted to  
20 be connected to the word line; and a second access transistor having  
21 a first active terminal connected to the output of the second inverter,  
22 having a second active terminal connected to the second bit line, and  
23 having a gate connected to the word line.

1 7. A static random access memory cell comprising:

2 a first inverter including a first p-channel pullup transistor, and  
3 a first n-channel pulldown transistor in series with the first p-channel  
4 pullup transistor;

5 a second inverter including a second p-channel pullup transistor,  
6 and a second n-channel pulldown transistor in series with the second  
7 n-channel pullup transistor, the first inverter being cross-coupled with  
8 the second inverter, the first and second pullup transistors sharing a  
9 common active area;

10 a first access transistor having an active terminal connected to the  
11 first inverter;

12 a second access transistor having an active terminal connected to  
13 the second inverter; and

14 an isolator isolating the first pullup transistor from the second  
15 pullup transistor.

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17 8. A static random access memory cell in accordance with  
18 claim 7 wherein the first and second pullup transistors have respective  
19 gates, wherein the common active area is shared by the gates of the  
20 first and second pullup transistors, and wherein the isolator isolates the  
21 gate of the first pullup transistor from the gate of the second pullup  
22 transistor.

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1 9. A static random access memory cell in accordance with  
2 claim 7 wherein the isolator comprises an isolation gate adapted to be  
3 biased to isolate the first pullup transistor from the second pullup  
4 transistor.

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6 10. A static random access memory cell in accordance with  
7 claim 9 wherein the isolation gate cooperates with the active area to  
8 define a p-channel transistor.

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10 11. A static random access memory cell in accordance with  
11 claim 10 wherein the gate of the isolator is connected to a voltage  
12 effective to tri-state the transistor.

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14 12. A static random access memory cell in accordance with  
15 claim 9 wherein the isolation gate cooperates with the active area to  
16 define a p-channel transistor, the gate of the isolator being connected  
17 to a positive voltage.

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19 13. A static random access memory cell in accordance with  
20 claim 8 wherein the first inverter has an output, and the active terminal  
21 of the first access transistor is connected to the output of the first  
22 inverter; and wherein the second inverter has an output, and the active  
23 terminal of the second access transistor is connected to the output of  
24 the second inverter.

1 14. A method of manufacturing a static random access memory  
2 cell including first and second cross-coupled invertors, each invertor  
3 including a p-channel transistor connected in series with an n-channel  
4 transistor, the p-channel transistors having sources that are connected to  
5 each other and that are adapted to be connected to a common first  
6 voltage, and the p-channel transistors having respective drains; the  
7 n-channel transistors having respective sources that are connected to  
8 each other and that are adapted to be connected to a common second  
9 voltage, lower than the first voltage, and the n-channel transistors having  
10 respective drains; the method comprising the following steps:

11 providing a silicon substrate;

12 defining the first and second invertors relative to the substrate  
13 such that the first and second invertors include an active area common  
14 to drains of the p-channel transistors; and

15 defining an isolation gate relative to the common active area,  
16 between the drains of the p-channel transistors.

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18 15. A method of manufacturing a static random access memory  
19 cell in accordance with claim 14 wherein the step of defining the  
20 isolation gate comprises using polysilicon to define the gate.  
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1 16. A method of manufacturing a static random access memory  
2 cell in accordance with claim 14 and further comprising the step of  
3 connecting the sources of the p-channel transistors to the first voltage,  
4 connecting the sources of the n-channel transistors to the second  
5 voltage, and connecting the isolation gate to a voltage higher than the  
6 second voltage.

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8 17. A method of manufacturing a static random access memory  
9 cell in accordance with claim 14 and further comprising the step of  
10 connecting the isolation gate to the first voltage.

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12 18. A method of manufacturing a static random access memory  
13 cell in accordance with claim 14 wherein the step of defining the  
14 isolation gate comprises forming polysilicon on the common active area.  
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1           19. A method of manufacturing a static random access memory  
2 cell in accordance with claim 14 wherein the first inverter has an  
3 output, and wherein the second inverter has an output, and further  
4 comprising the step of defining a first access transistor having a first  
5 active terminal connected to the output of the first inverter, having a  
6 second active terminal adapted to be connected to a first bit line, and  
7 having a gate adapted to be connected to a word line; and defining a  
8 second access transistor having a first active terminal connected to the  
9 output of the second inverter, having a second active terminal adapted  
10 to be connected to a second bit line, and having a gate adapted to be  
11 connected to the word line.



1           20. A method of manufacturing a wafer including a plurality of  
2 static random access memory cells, each cell including first and second  
3 cross-coupled invertors, each invertor including a p-channel transistor  
4 connected in series with an n-channel transistor, the p-channel transistors  
5 having sources that are connected together and that are adapted to be  
6 connected to a common first voltage, and having respective drains; the  
7 n-channel transistors having sources that are connected together and that  
8 are adapted to be connected to a common second voltage, lower than  
9 the first voltage, and having respective drains; the method comprising  
10 the following steps:

11           providing a silicon substrate;

12           defining active areas relative to the substrate for the static  
13 random access memory cells, the active areas including an active area  
14 having the general shape of a stepladder, including two parallel, spaced  
15 apart sides, and a plurality of parallel, spaced apart portions extending  
16 between the sides, such that the sides define drains of a plurality of  
17 the p-channel transistors; and

18           defining respective isolation gates relative to active areas, between  
19 the drains of the p-channel transistors within each static random access  
20 memory cell.

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22           21. A method of manufacturing a wafer in accordance with  
23 claim 20 wherein the step of defining the isolation gates comprises using  
24 polysilicon to define the gates.

1           22. A method of manufacturing a wafer in accordance with  
2 claim 20 and further comprising the step of connecting the sources of  
3 the p-channel transistors to the first voltage and connecting the sources  
4 of the n-channel transistors to the second voltage.

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6           23. A method of manufacturing a wafer in accordance with  
7 claim 22 and further comprising the step of connecting the isolation  
8 gates to a voltage higher than the second voltage.

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10          24. A method of manufacturing a wafer in accordance with  
11 claim 22 and further comprising the step of connecting the isolation  
12 gates to the first voltage.

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14          25. A method of manufacturing a wafer in accordance with  
15 claim 22 wherein the step of defining the isolation gates comprises  
16 forming polysilicon on the active area between the drains of the  
17 p-channel transistors of each static random access memory cell.

1        26. A method of manufacturing a wafer in accordance with  
2 claim 22 wherein, for each static random access memory cell, the first  
3 inverter has an output, and the second inverter has an output, the  
4 method comprising the step of defining a first access transistor, for each  
5 static random access memory cell, having a first active terminal  
6 connected to the output of the first inverter of that cell, having a  
7 second active terminal adapted to be connected to a bit line, and  
8 having a gate adapted to be connected to a word line; and defining a  
9 second access transistor, for each static random access memory cell,  
10 having a first active terminal connected to the output of the second  
11 inverter of that cell, having a second active terminal adapted to be  
12 connected to a bit line different from the first mentioned bit line, and  
13 having a gate adapted to be connected to the word line.